CLAIMS

1. An apparatus, comprising:

a capacitive structure, comprising:

a) an inner node, comprising:

a first pair of vertically aligned strips electrically connected with one or more vias, a second pair of vertically aligned strips electrically connected with one or more vias, the higher strips of both of said pairs at a same metal level, the lower strips of both of said pairs at a same lower metal level; and,

b) an outer node, comprising:

at said metal level:

a first metal structure having a pair of windows, a first of said windows surrounding and isolated from a first of said higher strips, a second of said windows surrounding and isolated from a second of said higher strips;

at said lower metal level:

a second metal structure having a pair of windows, a first of said windows surrounding and isolated from a first of said lower strips, a second of said windows surrounding and isolated from a second of said lower strips;

said first and second metal structures electrically connected with one or more vias.

2. The apparatus of claim 1 wherein said lower metal level is a second metal level of said semiconductor device and said higher metal level is a third metal level of said semiconductor device.

3. The apparatus of claim 1 further comprising a first plane of metal that is vertically aligned with and above said higher strips and said first metal structure.

4. The apparatus of claim 3 wherein said first plane of metal comprises shielding strips and is electrically connected to said outer node.

5. The apparatus of claim 4 further comprising a second plane of metal that is vertically aligned with and beneath said lower strips and said second metal structure, said second plane of metal being electrically connected to said outer node.

6. The apparatus of claim 5 wherein said second plane of metal comprises shielding strips.

7. The apparatus of claim 6 wherein said shielding strips of said second plane partially surround and are isolated from a bus formed at a same level as said second plane, said bus electrically connected to said inner node.

8. The apparatus of claim 6 further comprising a bus located along said metal layer and connecting said higher strips so as to be connected to said inner node.

9. The apparatus of claim 6 further comprising a bus located along said lower metal layer and connecting said lower strips so as to be connected to said inner node.

10. The apparatus of claim 1 wherein said capacitive structure is part of an Analog-to-Digital Converter (ADC) circuit.

11. An apparatus, comprising:

a capacitive structure comprising, at a same metal level, an outer metal feature that forms a window that completely surrounds and is isolated from an inner, rectangular metal strip that runs along a width of said capacitive structure .

12. The apparatus of claim 11 wherein said outer metal feature further comprises a second window that completely surrounds and is isolated from a second, inner, rectangular metal strip that runs along a width of said capacitive structure.

13. The apparatus of claim 11 further comprising, at another level and in a location that is vertically aligned with said outer metal feature, a second metal feature that is connected to said outer metal feature with one or more vias.

14. The apparatus of claim 12 further comprising, at said another level and in a location that is vertically aligned with said rectangular metal strip, a third metal feature that is connected to said rectangular metal feature with one or more vias and is isolated from said second metal feature.

15. The apparatus of claim 11 further comprising at another level and in a location that is vertically aligned with said outer metal feature, a second outer metal feature that forms a second window that completely surrounds and is isolated from a second inner rectangular metal strip that runs along a width of said capacitive structure along said another level, said second inner rectangular metal strip vertically aligned with said inner rectangular metal strip, said second outer metal feature electrically connected to said outer metal feature, said second inner rectangular metal strip electrically connected to said inner rectangular strip.

16. The apparatus of claim 15 wherein said features are vertically connected with vias.

17. The apparatus of claim 16 wherein said features are vertically connected with solid metal lines.

18. The apparatus of claim 11 wherein said capacitive structure is part of an ADC circuit.

19. A machine readable medium having stored thereon instructions which when executed by a computing system cause said computing system to perform a method, said method comprising:

designing a capacitive structure into a design for an electronic circuit, said capacitive structure comprising:

a) a first node, comprising:

a first pair of vertically aligned strips electrically connected with one or more vias, a second pair of vertically aligned strips electrically connected with one or more vias, the higher strips of both of said pairs at a same metal level, the lower strips of both of said pairs at a same lower metal level; and,

b) a second node, comprising:

at said metal level:

a first metal structure having a pair of windows, a first of said windows surrounding and isolated from a first of said higher strips, a second of said windows surrounding and isolated from a second of said higher strips;

at said lower metal level:

a second metal structure having a pair of windows, a first of said windows surrounding and isolated from a first of said lower strips, a second of said windows surrounding and isolated from a second of said lower strips;

said first and second metal structures electrically connected with one or more vias.